1.(currently amended) An apparatus to allow dual master control of a slave peripheral unit, comprising:

a first ~~and~~ master control unit able to provide a first plurality of control bits;

a second master control unit~~, each master control unit~~ able to provide a second plurality of control bits;

a slave peripheral unit operable under the control of ~~by~~ a resultant shared subset of the first and second plurality of control bits ~~from the master control units~~;

a slave peripheral interface coupled between the master control units and the slave peripheral unit, the interface ~~includes~~ including a data communication bus for carrying the control bits; and

a logic configuration block coupled to the communication bus, the logic configuration block ~~controls~~ controlling the generation of said resultant ~~access of the~~ shared subset of control bits ~~to~~ for the slave peripheral unit~~, the~~ according to a logical combination dynamically set by ~~block configurable by a set of~~ configuration bits ~~accessible by only a first~~from the first master control unit.

2.(previously presented) The apparatus of claim 1, wherein the configuration bits set logic configuration bits in the logic configuration block, the logic configuration bits defining the control of the common subset of shared control bits by the master control units.

3.(previously presented) The apparatus of claim 1, wherein the configuration bits set a logic operation in the logic configuration block, the logic operation operates on the shared control bits from the master control units to define a combined output set of control bits to control the peripheral.

4.(previously presented) The apparatus of claim 1, wherein the slave peripheral unit includes respective first and second input registers coupled to the first and second master control units through the communication bus, the input registers being coupled to provide the shared control bits from the master control units to the logic configuration block, and wherein the slave peripheral unit includes a configuration register accessible to the first master

control unit and coupled to provide configuration bits to the logic configuration block.

5.(currently amended) The apparatus of claim 4, wherein the second mastermain control unit is operable to read the configuration register to confirm accessibility of the slave peripheral unit by the second mastermain control unit.

6.(previously presented) The apparatus of claim 4, wherein the slave peripheral unit includes an output to output the logical combination of the shared control bits of the master control units from the logic configuration block.

7.(currently amended) The apparatus of claim 6, wherein the output is coupled to the shift input registers to output data back to the respective master control units.

8.(currently amended) The apparatus of claim 6, wherein the second mainmaster control unit is operable to read the output to confirm operability of the slave peripheral unit by the second mainmaster control unit.

9.(currently amended)- An apparatus to allow dual master control of a slave peripheral unit, comprising:

a first master control unit able to provide first control bits;

and a second master control unit, each master control unit able to provide second control bits;

a slave peripheral unit operable by a shared subset of the control bits from the master control units, the slave peripheral unit includes including respective first and second input registers tothat receive the first and second control bits from master control units and a configuration register accessible by the first master control unit;

a slave peripheral interface including a data communication bus coupled between the first and second master control units and the respective input registers of the slave peripheral unit, the communication bus for carrying the control bits; and

a logic configuration block coupled to the first and second input registers and the configuration register, the logic configuration block ~~controls~~ controlling generation ~~access~~ of the shared subset of control bits ~~to~~ for the slave peripheral unit, the logic block configurable by a set of configuration bits from the configuration register.

10.(previously presented) The apparatus of claim 9, wherein the configuration bits set a logic operation in the logic configuration block, the logic operation operates on the shared control bits from the master control units to define a combined output set of control bits to control the peripheral.

11.(currently amended) The apparatus of claim 9, wherein the second master~~main~~ control unit is operable to read the configuration register to confirm accessibility of the slave peripheral unit by the second master~~main~~ control unit.

12.(currently amended) The apparatus of claim 9, wherein the slave peripheral unit includes a output to output the logical combination of the shared control bits of the master control units from the logic configuration block, and wherein the second ~~main~~master control unit is operable to read the output to confirm operability of the slave peripheral unit by the second ~~main~~master control unit.

13.(currently amended) ~~The apparatus of claim 9, wherein~~ An apparatus to allow dual master control of a slave peripheral unit, comprising:

first and second master control units, each control unit able to provide control bits;

a slave peripheral unit operable by a shared subset of the control bits from the master control units, the slave peripheral unit including respective first and second input registers that receive the first and second control bits from master control units and a configuration register accessible by the first master control unit;

a slave peripheral interface including a data communication bus coupled between the first and second master control units and the respective input registers of the slave peripheral unit, the communication bus being ~~is~~ a serial bus and for carrying the control bits; and

a logic configuration block coupled to the input registers and the configuration register, the logic configuration block controlling access of the shared subset of control bits to the slave peripheral unit, the block configurable by a set of configuration bits from the configuration register.

14.(previously presented) A method of providing dual master control of a slave peripheral unit, the method comprising the steps of:

providing a first set of control bits and a set of logic configuration bits from a first master control unit, and providing a second set of control bits from a second master control unit;

configuring a logic operation in a combination logic block with the set of logic configuration bits;

performing the logical operation on the first and second set of control bits to provide a resultant set of control bits; and

applying the resultant control bits to a slave peripheral unit.

15.(previously presented) The method of claim 14, further comprising the step of reading the configuration bits by the second master unit to confirm accessibility of the slave peripheral unit.

16.(currently amended) A method of providing dual master control of a slave peripheral unit, the method comprising the steps of:

providing a first set of control bits and a set of logic configuration bits from a first master control unit, and providing a second set of control bits from a second master control unit;

configuring a logic operation in a combination logic block with the set of logic configuration bits;

performing the logical operation on the first and second set of control bits to provide a resultant set of control bits;

applying the resultant control bits to a slave peripheral unit; and

~~The method of claim 14, further comprising the step of~~ reading the resultant control bits by the second master unit to confirm operability of the slave peripheral unit.

17.(previously presented) The method of claim 14, wherein the providing step includes providing the control bits serially ~~in a common format~~.

18.(newly presented) A method of generating control bits for a slave peripheral unit responsive to bits from first and second master control units, the method comprising the steps of:

receiving a first set of bits and at least one logic configuration bit from the first master control unit;

receiving a second set of bits from the second master control unit;

configuring a logic operation responsive to said at least one logic configuration bit;

performing the logical operation on the first and second set of bits to selectively combine the bits according to the configured logic and generate a resultant set of bits; and

applying the resultant set of bits as control bits to the slave peripheral unit.

19.(newly presented) A slave device comprising:

a first input for first control bits generated by a first master control unit;

a second input for second control bits generated by a second master control unit; and

a combinational logic block responsive to logic configuration bits received from said first master control unit for configuring a dynamic logic combination of said first and second sets of bits, the combinational logic block outputting resultant control bits for the slave device derived from a combination of the first and second sets of bits.

20.(newly presented) The slave device of claim 19, further comprising first and second registers for the first and second control bits, the registers to provide first and second control bits from the first and second master control units to the combinational logic block.

21.(newly presented) The slave device of claim 19, further comprising a configuration register accessible to the first master control unit and coupled to provide configuration bits to the combinational logic block.